

BENCHMARKING LINEAR AND NON-LINEAR BEHAVIOUR OF POWER INDUCTORS FOR SWITCHED MODE POWER SUPPLIES

Markus MAKOSCHITZ

Austrian Institute of Technology (AIT)
Markus.Makoschitz@ait.ac.at

Jon BERROTARAN

Austrian Institute of Technology (AIT)
Jon.Berrotaran@ait.ac.at

Sumanta BISWAS

Austrian Institute of Technology (AIT)
Sumanta.Biswas@ait.ac.at

ABSTRACT

Basic power electronic circuits (such as e.g. a Buck, Boost, Buck-Boost or half-bridge topology) for grid connected applications are in general comprised of a voltage DC-link, two or more semiconductors and an LC input/output filter. The inductor is in general one of the more expensive and bulky parts and thus an optimized design is required in most network applications. Besides design parameters as volume, cost and frequency response, also a trade-off between low core losses, and maximum current excitation for critical operating conditions as e.g. overload capability exists. If the coil is not properly designed, the non-linear area of the inductor can be reached which results in faulty system operation of the device. Hence, a testbench conception is proposed in this paper, which allows to characterize both, linear and non-linear behaviour of power inductors for switched mode power supplies and/or network applications. Eventually, the prototypical setup and measurement results will be presented and compared to analytical results in order to verify the proper operation of the test system.

INTRODUCTION

The design of power electronic circuits and their components in general depends on their particular application (power supplies, network applications, motor drives, etc.) and required functionality. Those power conversion topologies typically consist of switches, capacitors (C) and inductors (L). Both passive components benefit from its ability to store electric and magnetic energy, respectively. In general, a combination of inductive and capacitive components serves as current filtering solution (e.g. single- or multistage LCL filters in classical voltage source converters). Thus, inductive components are typically involved in most kinds of power electronics circuits (half-bridge, full-bridge, multi-level/multi-cell topologies...) and tend to be the most expensive and bulky devices.

For a reliable power converter operation and performance, a proper design of the required inductive parts appears as a challenging task (as described in [1] for PV inverter systems) as in general a lot of parameters are just sparsely documented especially when it comes down to the transition between linear to non-linear areas of the implemented inductor [2-3]. Classical measurement devices as RLC meters are currently commercially available which however merely specify the small signal impedance of the device of interest. Such an impedance specification at different frequencies is usually performed at very low excitation

voltages and currents (typically mA- or V-range). Therefore, some critical parameters, as e.g. maximum current saturation and non-linear inductive behaviour cannot be evaluated with such an RLC impedance measurement device. Since in many power electronic circuits, chokes can be stressed by current levels from the ampere to kilo-ampere range a coil characterization device may come handy that can test those inductors with at least twice the operating current and determine and evaluate those critical operating areas such as effects according to non-linearity of the component. In [4] an energy storage approach is described on how to extract that non-linear inductance performance. However, no further information on prototypical information or detailed functionality has been provided so far. The following sections, thus focus on the conception of the testbench itself and provide some fundamental design considerations and guidelines as well as a basic understanding of the occurring sequence of a test cycle.

FUNDAMENTAL INDUCTIVE BEHAVIOUR

Most inductors in power electronic circuits consist of a defined number N of copper or aluminium windings a magnetic core of specific material (e.g. ferrite, amorphous alloys, etc.) and a specified air gap (as shown in Fig. 1) or distributed air gaps (powder core).

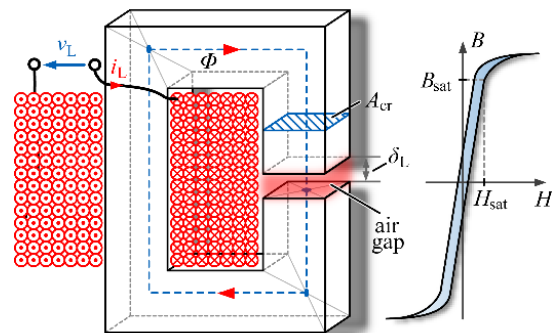


Fig. 1: (left) A basic implementation of a standard power inductor and (right) appropriate BH hysteresis curve of utilized magnetic core.

The biggest advantage of an inductor using magnetic materials compared to an air cored coil is the substantial reduction of the inductor volume that can be achieved for similar inductance values. The presence of a magnetic core introduces additional losses (dependent on material, [5]). Furthermore, all materials show a level of saturation which mainly relates to the BH-curve of the material and its instantaneous excitation. As long as the core material operates in the linear region, basic design inductor equations very well-known from literature are defined as follows:

$$\Phi(\mathcal{A}) = \int_{\mathcal{A}} B_n \cdot dA; \quad \Phi_v = N \cdot \Phi; \quad \Phi_v = L \cdot I;$$

$$\theta(\mathcal{C}) = \int_{\mathcal{C}} H_s \cdot ds = NI; \quad B = \mu H; \quad \mu_0 = 4\pi \cdot 10^{-7} \frac{Vs}{Am}$$

with θ the magnetomotive force, Φ the magnetic flux, B the magnetic flux density, H the magnetic field intensity, μ the permeability, L the inductance of the coil, and A the cross-section (further denoted as A_{cr}) of the magnetic core. In order to operate the inductor within the linear area of the material, the maximum occurring magnetic flux density B_{max} has to be lower than the saturated magnetic flux density B_{sat} ($B_{max} < B_{sat}$) which results in

$$B_{max} = \frac{|\Phi_{DC} + \Phi_{AC}|_{max}}{A_{cr}} < B_{sat} = \frac{LI_{sat}}{NA_{cr}}$$

The implemented testbench should help power electronic engineers to find those critical parameters as saturation current, inductance for different excitation levels, etc. utilizing a plug & play device.

TESTBENCH CONCEPTION

General Setup

Fig. 2 shows an overview of the concept of such a proposed measurement system.

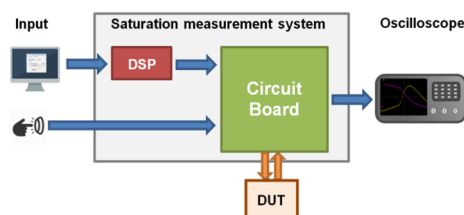


Fig. 2: Concept of the inductive measurement device.

In principle, the solution consists of 6 different parts:

- An **oscilloscope** for most important measurement signal evaluation (DC-link voltage, inductor current, inductor voltage,...). Relevant data can be extracted and analysed on external devices such as a PC or laptop with appropriate software (e.g. EXCEL, Matlab,...).
- The **power electronics circuit** comprises the DC-link capacitor bank, an IGBT half-bridge with dedicated gate drivers, power supplies, charging and discharging circuits, safety turn-off connections, as well as communication building blocks to be able to derive all signals that are sent by an external device.
- A digital signal processor (**DSP**) board which provides the interlink between power electronics hardware and an external software which is capable to generate “one-” or “multi-shot” events. It is important to note that the DSP board is only required if an external device is provided to manually set the turn-on pulse length and pulse repetition time of S_1 .
- If no such external device is utilized, a single shot can also be generated via a **push button (with appropriate debouncing circuits)** to allow the solution to be a “carry-on” “plug & play” device which doesn’t require

any additional software if not desired or available. An additional toggle switch facilitates to set the requested mode (DSP or push-button operation).

- The **device under test (DUT)** which in this case is the designed inductor of interest.

Maximum Excitation Capability

The maximum current capability of the system highly depends on the chosen semiconductor components. For the solution at hand, high current IGBTs have been utilized in order to allow an inductor characterization up to the hundreds of Amperes range. As a non-linear operation of the inductor is expected after the saturation point of the core is reached utilizing an IGBT becomes beneficial as there are several gate driver chips with integrated collector voltage desaturation detection and fault status feedback available on the market. The gate driver is observing the collector voltage (v_{CE}) of the IGBT during its on state. If v_{CE} exceeds a specific voltage limit the gate driver is returning a fault command and resetting the IGBT into a blocking state in order to prevent irreversible damage to the semiconductor. As the current of the inductor can ramp up after reaching the critical saturation limit uncontrollably steep a desaturation detection is mandatory. Alternatively, also a Si or silicon carbide (SiC) MOSFET could be used instead of an IGBT. In principle, a very similar protection circuit could be applied. However, the blanking time which is sufficient for an IGBT technology is typically too long for the MOSFET device. Due to the high achievable switching speed of MOSFETs (and dedicated evoked noise) there is a critical trade-off of the short circuit detection time as it should be long enough to ignore irrelevant noise but short enough to provide enough safety-relevant standards to prevent the device from detriment.

It has to be noted that the maximum current capability of the system can be easily extended if two or more semiconductors of the same type (e.g. IGBTs, MOSFETs,...) are paralleled and thus the system can be easily upgraded for testing currents in the high kiloampere range (which might be of interest for inductors for power converters >100kW).

OPERATING SEQUENCE

Basic Principle

The DUT is directly going to be connected to the main circuit board (illustrated in **Fig. 3**). It can be operated either manually via a push button (one shot) or via a DSP (multi-shot) controlled by an external software including a GUI.

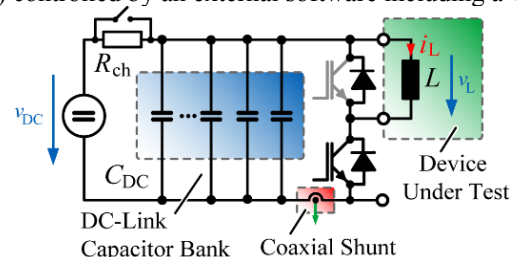


Fig. 3: Simplified schematic of proposed testbench.

The sequence of the solution is very similar to the classical double pulse test which is used in industry to characterize switching losses of power semiconductors. Expected current and push-button waveforms including linear and non-linear operating areas of the inductor are shown in Fig. 4.

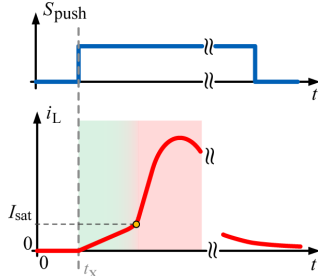


Fig. 4: Expected current waveform of the inductor according to the proposed solution.

The DC-link of the system gets charged via an external power supply and a charging resistor. The maximum current of the external power supply can be limited to very low current values (e.g. 0.1A) as it is only required during the charging process. During the “one-shot” event the effect of the power supply can be neglected. Thus, after the DC-link is fully charged the power supply can be even disconnected from the device. Moreover, the ratings of the power supply are defined by the maximum requested voltage for a specified stored energy within the capacitor. Thus, if a high amount of capacitance is implemented in the first place, the required DC-link voltage can be even $< 40V$. This is however dependent on the maximum expected inductor current i_L . Additionally, a power supply with low current capability is sufficient as the energy during the characterization process will be provided by the DC-link of the testbench and not by the external power supply. During the charging process of the DC-link switches S_1 and S_2 are turned OFF. The DUT is connected between both output connectors (hence parallel to S_2) and is floating during that turn-OFF cycle of S_1 & S_2 . The energy stored in the DC-link capacitor bank is equal to

$$W_C = \frac{1}{2} CV^2.$$

Apparently, while the stored energy only increases straight-proportional with additional capacitance, it is ascending with x^2 for increasing voltage levels. Therefore, depending on the utilized capacitance of the DC-link the voltage should be set accordingly in order to omit an unnecessary malfunction due to excessive current stress of the implemented IGBT. Furthermore, there is an additional degree of optimization in terms of volume of the testbench as far as there would be a stringent volume related requirement for such a test system.

The current i_L will be measured by a coaxial shunt (which introduces some small amount of additional resistance and parasitic inductance). The negative bus of the DC-link can be grounded. Thus, the coaxial shunt placed between negative DC-link busbar and low-side IGBT is not exposed to any high switching voltage transitions and can therefore be directly connected to the scope. The voltage of the inductor

has to be measured via a differential voltage probe. Measurement data of both voltage and current probes can be displayed and recorded via the scope.

LC Resonant Circuit Principle

The following subsections will give a short discussion on occurring phenomena as they appear during a test-cycle of the proposed device (simplified circuit illustrated in Fig. 5(left)). For sake of simplicity, a linear inductor and ideal characteristics of IGBT and diode are assumed.

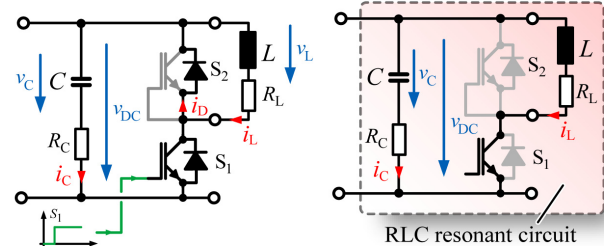


Fig. 5: (left) Simplified test circuit including resistive shares of capacitors and inductors. (right) Current path while S_1 is turned ON and S_2 remains in OFF state.

If the low-side IGBT is turned ON (cf., Fig. 5(right)), the whole energy stored within the DC-link will be transferred directly to the inductor. If no parasitic resistive shares and no IGBTs and or diodes would be present the circuit would resonate at a frequency $f_s = 1/(2\pi\sqrt{LC})$ which is illustrated in an uZi diagram as shown in Fig. 6.

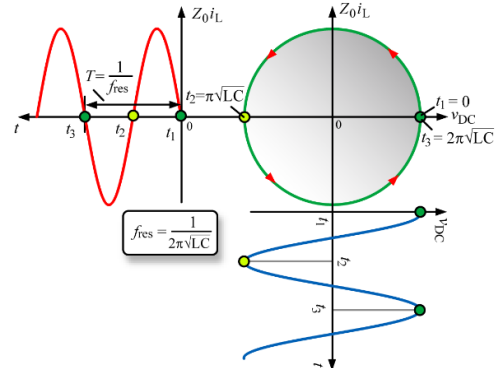


Fig. 6: uZi diagram of an LC resonant tank.

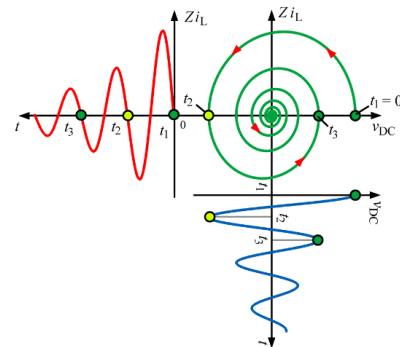


Fig. 7: uZi diagram of an RLC resonant circuit.

RLC Resonant Circuit Principle

Due to the presence of parasitic resistive shares (parasitic resistance of capacitors, inductors, power traces, turn-on

resistance of IGBT and diodes), parts of the initially stored energy get continuously depleted and the oscillation decays (cf., Fig. 7).

It has to be noted that under presence of parasitic and real resistors, the maximum of the inductor current i_L no longer appears at $v_C = 0$ ($t = t_3$) but at $v_C > 0$ ($t = t_2$).

RLC Resonant Circuit Principle incl. IGBT & D

If now IGBTs (and diodes) are considered, neither the DC-link voltage nor the inductor current can enter the remaining quadrants 2-4 of the uZi diagram as the diode of S_2 will immediately conduct if $v_{DC} = 0$ (see Fig. 8). From $t_1 \dots t_3$ v_C and i_L conform to resonant behaviour appropriately.

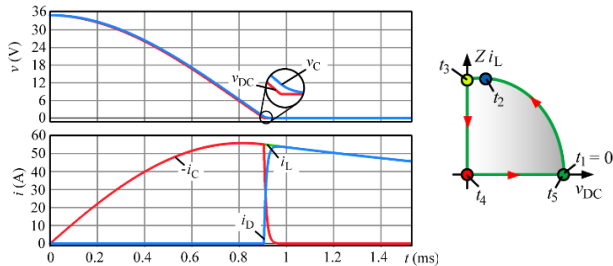


Fig. 8: (left) voltage and current waveforms of proposed test system assuming ideal power semiconductor (diode & IGBT). (right) Dedicated uZi diagram.

According to Kirchoff's law and if all differential equations are properly derived, the i_L and v_C can be derived for $t = t_1 \dots t_3$ and calculate to

$$v_C(t) = V_{init} e^{-\frac{t}{\tau_L}} \left[\cos(\omega_r t) + \frac{1}{\omega_r \tau_L} \sin(\omega_r t) \right]$$

$$i_L(t) = C V_{init} \left[\omega_r + \frac{1}{\omega_r \tau_L^2} \right] e^{-\frac{t}{\tau_L}} \sin(\omega_r t)$$

whereas ω_r results in

$$\omega_r = \frac{\sqrt{1 - \frac{(R_L + R_C)^2 C}{4L}}}{\sqrt{LC}} \quad \text{for} \quad \frac{(R_L + R_C)^2 C}{4L} < 1$$

And τ_L yields $\tau_L = 2L/(R_L + R_C)$. It has to be noted that S_1 is still turned ON. At $t = t_3$ the diode of S_2 starts conducting and two short circuits are formed (illustrated in Fig. 9).

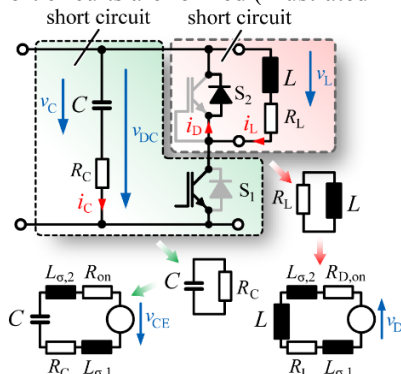


Fig. 9: Equivalent circuit during the occurring discharging process ($t = t_3 \dots t_4$) of both, DC-link and inductor.

Thus, the oscillating process is immediately interrupted and i_L is decreasing as L gets discharged according to $\tau_L = L/R_L$. Furthermore, as there is also some small amount

of energy still stored in capacitor C , it will also be discharged. However, the process is defined by the parasitic resistance of the capacitor itself pursuant to $\tau_C = R_C \cdot C$.

Therefore, the current of the high-side diode is defined via both discharging events and can be computed by $i_D = i_L + i_C$. Thus, the process that can be observed in Fig. 8 at $t \sim 0.8$ ms is not a classical S_1 to S_2 current commutation as known from hard switching half-bridge topologies (as S_1 is still conducting). If S_1 would be turned OFF during $i_C \neq 0$ and $i_L \neq 0$ the current is forced to directly commutate to D_2 and the di/dt is mainly driven via parasitic inductive shares within the circuit (e.g. DC-link power loop, etc.).

If collector voltage v_{CE} , on-resistor R_{on} of IGBTs and forward voltage v_D and on-state resistance $R_{D,on}$ of diode D_2 will be considered as non-ideal anymore a slight swing-back into all 3 remaining quadrants (uZi diagram) can be observed. If rather small voltages of v_{DC} are applied in order to set the test cycle it is preferred to utilize a MOSFET instead of the IGBT in order to omit the collector voltage v_{CE} . Additionally, the discharging events are adapted due to the presence of $R_{D,on}$ and R_{on} for inductive and capacitive discharging, respectively (equivalent circuit shown in Fig. 9 (bottom)). However, even if the analytic equations increase in complexity due to non-linear voltages v_{CE} and v_D , the general sequence as previously discussed still perpetuates. The whole coil characterisation process (S_1 permanently turned ON) is illustrated in Fig. 10.

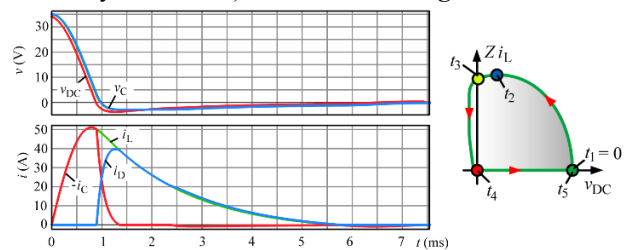


Fig. 10: (left) voltage and current waveforms of proposed test system assuming real active and passive components (L , C , diode, IGBT, ...). (right) Dedicated uZi diagram.

After the discharging process is finished and S_1 is turned OFF again at $t = t_4$, the external power supply can recharge the DC-link again to its initial voltage V_{init} from t_1 .

System behaviour due to saturating inductor

If a real inductor is now considered including a non-linear region after reaching I_{sat} , the discussed characterization sequence is still the same. Merely the inductor current will sharply increase after reaching I_{sat} .

Multifunctional Operation

It has to be noted, that after obtaining all data for a proper coil characterization, the system can be easily extended to serve as switched mode power converter setup (as shown in Fig. 11).

This allows to directly test the coil under more realistic conditions (S_1 and S_2 turned ON and OFF with switching frequency f_s) as utilized in e.g. half-bridge configurations whilst extending the output of the device with the inductor

of interest including an additional filter capacitor and (optional) a decent load. The switching frequency of S_1 and S_2 is limited appropriate cooling concept (not required if only “one-shot” operations are executed).

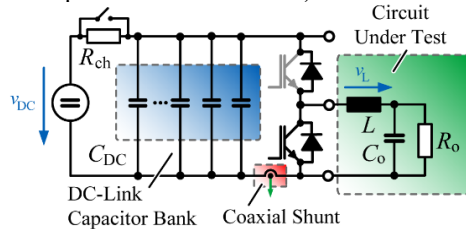


Fig. 11: Simplified schematic of testbench for inductor testing within integrated switched mode power converter.

EXPERIMENTAL RESULTS

The prototypical test bench is depicted in **Fig. 12** including all components as discussed in section “testbench conception”.

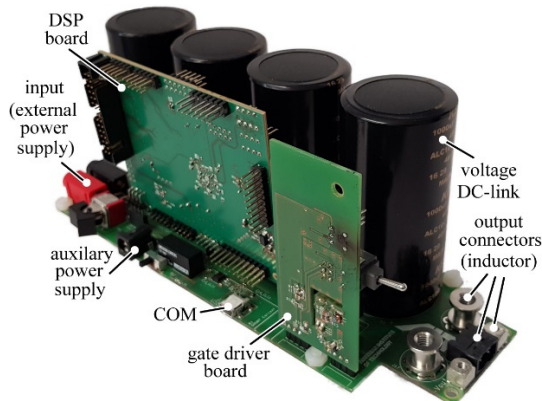


Fig. 12: Laboratory prototype of measurement device.

A wide range of inductive components are available for different kind of applications and some of them are chosen for an in-depth behaviour analysis of the core materials [6-7]. Three different inductors have been utilized:

- Licalloy GLT120D1511001A, $L_{0A} = 150\mu\text{H}$, $I = 10 A_{\text{nom}}$, $R_{\text{cu}} = 23 \text{ m}\Omega$,
- Ferrite ETD 49/25/16, N87 ungapped, designed air gap 1mm, $N = 26\text{wdg}$, $d_{\text{cu}} = 1 \text{ mm}$
- xFlux 0078615A7, $A_L = 82 \text{ nH}$, $N = 63\text{wdg}$, $d_{\text{cu}} = 1 \text{ mm}$

Measurement results of the inductor current i_L are plotted in **Fig. 13 (top)** and appropriate calculated inductance dependency on increasing current excitation is illustrated in **Fig. 13 (bottom)**. As can be seen ferrite shows a steep current ramp (saturation) after $\sim 60 \mu\text{s}$. The inductance of the licalloy cored coil exhibits very smooth saturation transition and no abrupt current slope can be observed as e.g. for ferrite. xFlux comes with a very high saturating magnetic flux density. The core is hence still in a linear region for $t < 200 \mu\text{s}$. Thus, xFlux is becomes beneficial for applications where a high overcurrent capability is required. However, it is limited in terms of iron losses if the power electronics system strives for a high switching frequency. The measurement equipment that has been used for i_L , v_L

and $v_{\text{GS,IGBT}}$ recordings are a Tektronix MSO 5 oscilloscope (1GHz Bandwidth) for high resolution measurements, a coaxial shunt (0.01478Ω), a passive voltage probe TPP1000 and a differential voltage probe THDP0200.

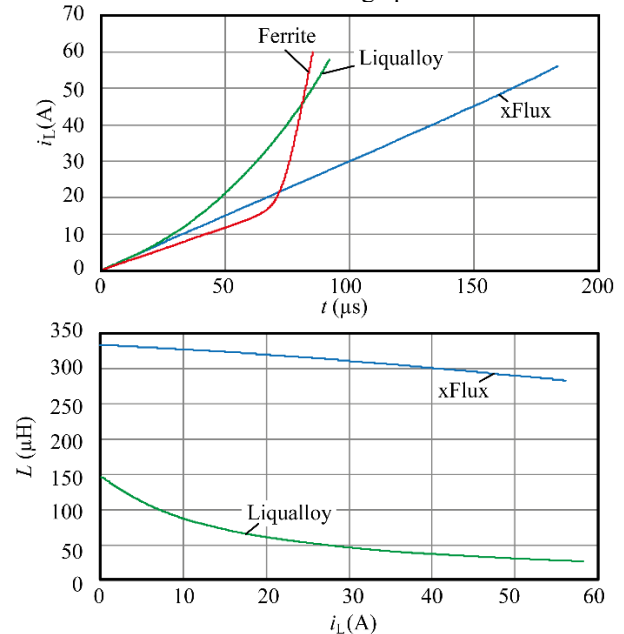


Fig. 13: (Top) Measured i_L for different magnetic cores after S_1 is closed at $t = 0$. (Bottom) Calculated inductance dependent on measured values of v_L and i_L .

CONCLUSION

A multifunctional test setup that allows to extract and evaluate different inductive core material properties (which typically cannot be determined with standard RLC meters) is discussed, analysed and implemented. Both, linear and non-linear behaviour of power inductors for switched mode power supplies and/or network applications can be addressed while using the discussed test system.

REFERENCES

- [1] J. Viinamäki, et al., 2015, “Effect of inductor saturation on the harmonic currents of grid-connected three-phase VSI in PV application”, ECCE Asia.
- [2] R. A. Salas, et al., 2008, “Nonlinear saturation modeling of magnetic components with an RM-type core, IEEE transactions on magnetics, vol. 44.
- [3] Y. Shiraki, et al., 2018, “Inductance analysis for compact dual-mode choke considering magnetic saturation”, IEEE EMC Europe, 630-635.
- [4] M. K. Meena, et al., 2011, “Nonlinear inductance measurement using an energy storage approach”, international symposium on electronic system design.
- [5] A. Ayachit, et al., 2016, “Steinmetz equation for gapped magnetic cores”, IEEE magnetics letters, vol. 7.
- [6] A. Williams, 2011, Fundamentals of magnetics design, IEEE [Online], 30-84.
- [7] H. Skarrie, 2001, “Design of powder core inductors”, Lund Institute of Technology: ISBN: 91-88934-19-5.